Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**(SIDE VIEW)**

**ANODE**

**.055**

**.081”**

**.090”**

**.090”**

**Top Material: Ag**

**Backside Material: Ag**

**Bond Pad Size: .055” X .055”**

**Backside Potential: ANODE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .090” X .090” DATE: 7/18/18**

**MFG: SENSITRON THICKNESS .027” P/N: SD090SA30**

**DG 10.1.2**

#### Rev B, 7/1